LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a display device, and more particularly to an active-matrix type liquid crystal display device.

2. DESCRIPTION OF THE RELATED ART

In an active-matrix type liquid crystal display device, on a liquid-crystal-side surface of one of respective substrates which face each other in an opposed manner with liquid crystal therebetween, for example, gate signal lines which extend in the x direction and are arranged in parallel in the y direction and drain signal lines which extend in the y direction and are arranged in parallel in the x direction are formed, regions which are surrounded by these respective signal lines constitute pixel regions, and a mass of these respective pixel regions arranged in a matrix array forms a liquid crystal display part.

Here, each pixel region includes a switching element which is driven in response to a scanning signal from one gate signal line and a pixel electrode to which a video signal is supplied from one drain signal line through the switching element.

The pixel electrode generates an electric field between the pixel electrode and a counter electrode which is formed on the above-mentioned one substrate or another substrate and

the optical transmissivity of the liquid crystal is controlled based on the electric field.

The optical transmissivity of the liquid crystal is determined based on an amount of potential difference (gray scale) of the video signal (voltage) applied to the pixel electrode with respect to the reference signal (voltage) applied to a counter electrode. Here, for example, for preventing the polarization of the liquid crystal, there has been known a method which generates a positive-side gray scale voltage and a negative-side gray scale voltage with respect to the above-mentioned video signal and applies these gray scale voltages alternately, for example.

In such a pixel driving, while there has been known a method in which a center voltage of the video signal is always fixed irrespective of an amplitude of the signal as shown in Fig. 12(a), there has been also known a method in which the center voltage of the video signal is decreased corresponding to the increase of the amplitude of the signal as shown in Fig. 12(b).

That is, the pixel is configured to be driven by forming the respective gray scale voltages such that an average value of the positive-side gray scale voltage and the negative-side gray scale voltage is increased with respect to the reference signal supplied to the counter electrode along with the decrease of the signal amplitude of the video signal (see Japanese

Unexamined Patent Publication Hei7(1995)-92937 (patent literature 1)).

BRIEF SUMMARY OF THE INVENTION

However, in the liquid crystal display device having such a constitution, when the signal amplitude of the video signal is switched between the maximum and the minimum, to be more specific, when the display is switched from black to white or from white to black, as can be readily understood from the drawing, the large difference arises between the center voltage before switching and the center voltage after switching.

This implies that when the observation is made in view of a state after switching, the state is equivalent to a state in which a DC current is applied between the pixel electrode of the pixel and the counter electrode until a point of time immediately before switching.

After switching, the center voltage suitable as a value after switching is applied by a switching element and hence, there exists no DC current between the pixel electrode of the pixel and the counter electrode. However, the response of liquid crystal molecules in response to the change of voltage requires several tens ms and hence, the above-mentioned influence of the DC current remains optically until the completion of the response.

Accordingly, there arises a phenomenon that the apparent

response speed is delayed due to the influence of the DC voltage.

The present invention has been made under such circumstances and it is an advantage of the present invention to provide a display device which can enhance a response speed.

To briefly explain the typical inventions among inventions disclosed in this specification, they are as follows. Means 1.

A display device according to the present invention, for example, includes a pixel electrode to which a video signal is supplied and a counter electrode to which a reference signal which becomes the reference with respect to the video signal is supplied in each pixel, wherein

a positive-side gray scale voltage and a negative-side gray scale voltage are formed with respect to the reference signal applied to the counter electrode such that

an average value of the positive-side gray scale voltage and the negative-side gray scale voltage is increased when a signal amplitude of the video signal falls in a range from a minimum value to a first value,

the average value of the positive-side gray scale voltage and the negative-side gray scale voltage is decreased when the signal amplitude of the video signal falls in a range from the first value to a second value, and

the average value of the positive-side gray scale voltage and the negative-side gray scale voltage is increased when the

signal amplitude of the video signal falls in a range from the second value to a maximum value.

Means 2.

The display device according to the present invention is, for example, on the premise of the constitution of means 1, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage with respect to the signal amplitude of the video signal assumes an upper extreme point at a point where the average value changes from the increase to the decrease and a lower extreme point at a point where the average value changes from the decrease to the increase in the range from the minimum value to the maximum value of the signal amplitude of the video signal.

Means 3.

The display device according to the present invention is, for example, on the premise of the constitution of means 2, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage with respect to the signal amplitude of the video signal which reaches the lower extreme point from the upper extreme point is changed monotonously.

Means 4.

The display device according to the present invention is, for example, on the premise of the constitution of means 2, characterized in that the average value of the positive-side

gray scale voltage and the negative-side gray scale voltage with respect to the signal amplitude of the video signal is changed monotonously from the minimum value to the upper extreme point of the signal amplitude of the video signal and from the lower extreme point to the maximum value of the signal amplitude of the video signal.

Means 5.

The display device according to the present invention is, for example, on the premise of the constitution of means 4, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal at the minimum signal amplitude of the video signal is smaller than the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal at the lower extreme point.

Means 6.

The display device according to the present invention is, for example, on the premise of the constitution of means 4, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal at the maximum signal amplitude of the video signal is larger than the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal

at the upper extreme point.

Means 7.

A display device according to the present invention, for example, includes a pixel electrode to which a video signal is supplied and a counter electrode to which a reference signal which becomes the reference with respect to the video signal is supplied in each pixel, wherein

a positive-side gray scale voltage and a negative-side gray scale voltage are formed with respect to the reference signal applied to the counter electrode such that

an average value of the positive-side gray scale voltage and the negative-side gray scale voltage is increased when a display gray scale of the video signal falls in a range from a minimum value to a first value,

the average value of the positive-side gray scale voltage and the negative-side gray scale voltage is decreased when the signal amplitude of the video signal falls in a range from the first value to a second value, and

the average value of the positive-side gray scale voltage and the negative-side gray scale voltage is increased when the display gray scale of the video signal falls in a range from the second value to a maximum value.

Means 8.

The display device according to the present invention is, for example, on the premise of the constitution of means

7, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage with respect to the signal amplitude of the video signal assumes an upper extreme point at a point where the average value changes from the increase to the decrease and a lower extreme point at a point where the average value changes from the decrease to the increase in the range from the minimum value to the maximum value of the display gray scale of the video signal.

Means 9.

The display device according to the present invention is, for example, on the premise of the constitution of means 8, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage with respect to the signal amplitude of the video signal which reaches the lower extreme point from the upper extreme point is changed monotonously.

Means 10.

The display device according to the present invention is, for example, on the premise of the constitution of means 9, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal at the minimum display gray scale of the video signal is smaller than the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal

at the lower extreme point.

Means 11.

The display device according to the present invention is, for example, on the premise of the constitution of means 9, characterized in that the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal at the maximum display gray scale of the video signal is larger than the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the signal amplitude of the video signal at the upper extreme point.

Means 12.

The display device according to the present invention is, for example, on the premise of the constitution of means 11, characterized in that the display device is driven in a normally white mode in which the minimum of the display gray scale assumes a white display and the maximum of the display gray scale assumes a black display.

Means 13.

The display device according to the present invention is, for example, on the premise of the constitution of means 11, characterized in that the display device is driven in a normally black mode in which the minimum of the display gray scale assumes a black display and the maximum of the display gray scale assumes a white display.

Means 14.

A display device according to the present invention, for example, includes a pixel electrode to which a video signal is supplied and a counter electrode to which a reference signal which becomes the reference with respect to the video signal is supplied in each pixel, wherein

with respect to the reference signal which is applied to the counter electrode,

along with the increase of an amplitude of the video signal voltage, a positive-polarity voltage of the video signal includes at least two points of inflection such that the positive-polarity voltage is sharply increased, is gradually increased and is again sharply increased, and a negative-polarity voltage of the video signal includes at least two points of inflection such that the negative-polarity voltage is gently decreased, is sharply decreased and is again gently decreased.

Means 15.

A display device according to the present invention, for example, includes a pixel electrode to which a video signal is supplied and a counter electrode to which a reference signal which becomes the reference with respect to the video signal is supplied in each pixel, wherein

along with the increase of a gray scale to be displayed, a positive-polarity voltage of the video signal includes at

least two points of inflection such that the positive-polarity voltage is sharply increased, is gradually increased and is again sharply increased, and a negative-polarity voltage of the video signal includes at least two points of inflection such that the negative-polarity voltage is gently decreased, is sharply decreased and is again gently decreased.

Means 16.

The display device according to the present invention is, for example, on the premise of the constitution of either one of means 1 or 7, characterized in that a circuit which forms the respective gray scale voltages includes gray scale division resistances and these resistances are constituted of seven or more resistances.

Means 17.

The display device according to the present invention is, for example, on the premise of the constitution of means 16, characterized in that a resultant resistance of the gray scale voltages between positive-polarity voltage outputs is set larger than a resultant resistance of the gray scale voltages between negative-polarity voltage outputs.

Means 18.

A driving method of a display device according to the present invention, for example, which includes a pixel electrode to which a video signal is supplied and a counter electrode to which a reference signal which becomes the reference with

respect to the video signal is supplied in each pixel, wherein

a positive-side gray scale voltage and a negative-side gray scale voltage are formed with respect to the reference signal applied to the counter electrode such that

an average value of the positive-side gray scale voltage and the negative-side gray scale voltage is increased when a signal amplitude of the video signal falls in a range from a minimum value to a first value,

the average value of the positive-side gray scale voltage and the negative-side gray scale voltage is decreased when the signal amplitude of the video signal falls in a range from the first value to a second value, and

the average value of the positive-side gray scale voltage and the negative-side gray scale voltage is increased when the signal amplitude of the video signal falls in a range from the second value to a maximum value.

The present invention is not limited to the above-mentioned constitutions and various modifications are conceivable without departing from the technical concept of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a graph showing one embodiment of the relationship between a signal amplitude of a video signal and a center voltage (an average value of a positive-side gray scale

voltage and a negative-side gray scale voltage) of the video signal of a display device according to the present invention;

Fig. 2 is a graph showing the relationship between the signal amplitude of the video signal and the display brightness of the display device according to the present invention;

Fig. 3 is a graph showing another embodiment of the relationship between the signal amplitude of the video signal and the center voltage (the average value of the positive-side gray scale voltage and the negative-side gray scale voltage) of the video signal of the display device according to the present invention;

Fig. 4 is a timing chart showing the video signal (having the positive-side gray scale voltage and the negative-side gray scale voltage), a scanning signal and a reference signal supplied to pixels of the display device according to the present invention;

Fig. 5 is a circuit diagram showing one embodiment of a resistance voltage divider circuit provided to a latter stage of a gray scale generating circuit provided to the display device according to the present invention;

Fig. 6 is a graph showing one embodiment of a video signal (having a positive-side gray scale voltage and a negative-side gray scale voltage) supplied to pixels of the display device according to the present invention in view of the relationship thereof with a display gray scale of the video signal;

Fig. 7 is a table showing one embodiment of respective resistance values of the resistance divider circuit in the latter stage of the gray scale generating circuit provided to the display device according to the present invention, gray scale voltages obtained from the resistance voltage divider circuit and the center voltage of the video signal;

Fig. 8 is an equivalent circuit diagram showing one embodiment of the display device according to the present invention;

Fig. 9 is a constitutional view showing one embodiment of the pixel of the display device according to the present invention;

Fig. 10 is a constitutional view showing another embodiment of the pixel of the display device according to the present invention;

Fig. 11 is a constitutional view showing one embodiment of a pixel of a liquid crystal display device according to the present invention; and

Fig. 12 is a graph showing an example of the relationship between a signal amplitude of a video signal and a center voltage of the video signal of a conventional liquid crystal display device.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of a display device according to the present

invention are explained in conjunction with drawings hereinafter.

Embodiment 1.

<<Overall equivalent circuit>>

Fig. 8 is an equivalent circuit diagram showing one embodiment of a display device (a liquid crystal display device in this embodiment) according to the present invention. Although the drawing is the equivalent circuit diagram, it is depicted in accordance with an actual arithmetic arrangement of the circuit of the display device.

The display device includes a pair of transparent substrates SUB1, SUB2 which are arranged to face each other in an opposed manner with liquid crystal therebetween, wherein the liquid crystal is sealed by a sealing material SL which also performs a function of fixing another transparent substrate SUB2 to one transparent substrate SUB1.

On a liquid-crystal-side surface of one transparent substrate SUB1 which is surrounded by the sealing material SL, gate signal lines GL which extend in the x direction and are arranged in parallel in the y direction and drain signal lines DL which extend in the y direction and are arranged in parallel in the x direction are formed.

Regions which are surrounded by the respective gate signal lines GL and the respective drain signal lines DL constitute pixel regions and a mass of these respective pixel regions in

a matrix array constitutes a liquid crystal display part AR.

Further, in the respective pixel regions which are arranged in parallel in the x direction, a common counter voltage signal line CL which runs in the inside of the respective pixel regions is formed. The counter voltage signal line CL constitutes a signal line for supplying a voltage which becomes the reference with respect to a video signal to a counter electrode CT of the pixel region described later.

In each pixel region, a thin film transistor TFT which is driven in response to a scanning signal from the one-side gate signal line GL and a pixel electrode PX to which a video signal is supplied from the one-side drain signal line DL via this thin film transistor TFT are formed.

This pixel electrode PX generates an electric field between the pixel electrode PX and a counter electrode CT which is connected to the counter voltage signal line CL and controls the optical transmissivity of the liquid crystal in response to the electric field.

Here, a capacitive element Cstg is formed between the pixel electrode PX and the counter voltage signal line CL and a video signal which is supplied to the pixel electrode PX is held for a relatively long time due to this capacitive element Cstg.

Respective ends of the above-mentioned gate signal lines GL extend beyond the above-mentioned sealing material SL and

the extended ends thereof form terminals GLT to which output terminals of the scanning signal drive circuit V are connected. Further, to input terminal of the scanning signal drive circuit V, a signal from a printed circuit board (not shown in the drawing) which is arranged outside the liquid crystal display panel is inputted.

The scanning signal drive circuit V is formed of a plurality of semiconductor devices. A plurality of gate signal lines GL which are arranged close to each other are formed into a group and one semiconductor device is allocated to each group of gate signal lines GL.

In the same manner, respective ends of the drain signal line DL extend beyond the sealing material SL and the extended ends constitute terminals DLT to which output terminals of the video signal drive circuit He are connected. Further, to input terminals of the video signal drive circuit He, a signal from a printed circuit board (not shown in the drawing) which is arranged outside the liquid crystal display panel is inputted.

The video signal drive circuit He is also formed of a plurality of semiconductor devices. A plurality of drain signal lines DL which are arranged close to each other are formed into a group and one semiconductor device is allocated to each group of drain signal lines DL. Further, the counter voltage signal lines CL are connected in common to a connection line at the right side in the drawing and the connection line

extends beyond the sealing material SL and constitutes a terminal CLT at an extended end thereof. From the terminal CLT, a voltage which becomes the reference with respect to the video signal is supplied to the pixels.

The respective gate signal lines GL are selected sequentially one after another in response to the scanning signal from the scanning signal drive circuit V.

Further, to respective drain signal lines DL, the video signal is supplied from the video signal drive circuit He at the timing of selecting the gate signal lines GL.

In the above-mentioned embodiment, the scanning signal drive circuit V and the video signal drive circuit He are constituted of semiconductor devices which are mounted on the transparent substrate SUB1. However, the scanning signal drive circuit V and the video signal drive circuit He may be formed of semiconductor devices of a so-called tape carrier method which are connected to each other while striding over the transparent substrate SUB1 and a printed circuit board, for example. Alternatively, when a semiconductor layer of the thin film transistor TFT is formed of a polycrystalline silicon (p-Si), semiconductor elements made of polycrystalline silicon may be formed on a surface of the transparent substrate SUB1 together with wiring layers.

<< Constitution of pixel >>

Fig. 9(a) is a plan view showing one embodiment of the

specific constitution of the above-mentioned pixel, Fig. 9(b) is a cross-sectional view taken along a line b-b in Fig. 9(a), and Fig. 9(c) is a cross-sectional view taken along a line c-c in Fig. 9(a).

First of all, on a liquid-crystal-side surface of the transparent substrate SUB1, a semiconductor layer LTPS formed of a polysilicon layer, for example, is formed. The semiconductor layer LTPS is formed by polycrystalizing an amorphous Si film formed by a plasma CVD device, for example, using an excimer laser.

The semiconductor layer LTPS is a semiconductor layer of the thin film transistor TFT and is formed in a roundabout manner such that the semiconductor layer LTPS traverses the gate signal line GL described later twice.

Further, on the surface of the transparent substrate SUB1 on which the semiconductor layers LTPS are formed, a first insulation film INS made of SiO_2 or SiN, for example, is formed such that the first insulation film INS also covers the semiconductor layers PS. The first insulation film INS is configured to function as gate insulation films of the thin film transistors TFT.

Further, on an upper surface of the first insulation film INS, the gate signal lines GL which extend in the x direction and are arranged in parallel in the y direction in the drawing are formed and the gate signal lines GL define rectangular pixel

regions together with the drain signal lines DL described later.

The gate signal lines GL are configured to run such that the gate signal lines GL traverse the semiconductor layer LTPS twice and portions of the gate signal lines GL which traverse the semiconductor layer LTPS function as gate electrodes of the thin film transistors TFT.

After the formation of the gate signal lines GL, impurities ions are implanted by way of the first insulation film INS so as to make regions of the semiconductor layer LTPS except for a region right below the gate signal line GL conductive thus forming a source region and a drain region of the thin film transistor TFT.

Further, on an upper surface of the first insulation film INS, counter electrodes CT are formed. With respect to the counter electrodes CT, for example, two strip-like electrodes which extend in the y direction in the drawing are arranged close to the drain signal lines DL described later in the pixel. These respective counter electrodes CT are integrally formed with a counter voltage signal line CL which runs in the x direction in the drawing at the substantially center of the pixel and the reference signal is supplied through the counter voltage signal line CL.

Further, on the upper surface of the above-mentioned first insulation film INS, a second insulation film which is made of SiO_2 or SiN, for example, is formed such that the second

insulation film GI also covers the gate signal lines GL and the counter electrodes CT (counter voltage signal lines CL).

On a surface of the second insulation film GI, the drain signal lines DL which extend in the y direction and are arranged in parallel in the x direction are formed. Then, portions of the drain signal lines DL are connected to the above-mentioned semiconductor layers LTPS via through holes TH1 which penetrate the second insulation film GI and the first insulation film INS disposed below the drain signal lines DL. Portions of the semiconductor layers LTPS which are connected with the drain signal lines DL are portions which constitute one region, for example, drain regions of the thin film transistors TFT.

On the surface of the second insulation film GI, a third insulation film PAS is formed such that the third insulation film PAS also covers the drain signal lines DL. On a surface of the third insulation film PAS, pixel electrodes PX are formed. These pixel electrodes PX are formed of strip-like electrodes which extend in the y direction in the drawing at the center of the pixels and hence, the pixel electrode PX is positioned between the above-mentioned respective counter electrodes CT. The pixel electrode PX has a portion thereof connected with another region, for example a source region of the thin film transistor TFT via a through hole TH2 which is formed in the third insulation film PAS, the second insulation film GI and the first insulation film INS disposed below the pixel electrode

in a penetrating manner.

Here, the pixel electrode PX is formed to have a large width at a portion thereof which intersects the counter voltage signal line CL and a capacitive element Cstg is formed between the pixel electrode PX and the counter voltage signal line CL at the portion.

Electric fields which have components parallel to the transparent substrate SUB1 are generated between the pixel electrode PX and the respective counter electrodes which are respectively positioned at both sides of the pixel electrode PX and the optical transmissivity of the liquid crystal can be controlled due to these electric fields.

Here, the pixel electrode PX is, in this first embodiment, formed of a light-transmitting conductive layer such as ITO (Indium Tin Oxide), ITZO (Indium Tin Zinc Oxide), IZO (Indium Zinc Oxide), SnO_2 (Tin Oxide), In_2O_3 (Indium Oxide), for example, for enhancing a numerical aperture.

Here, in the above-mentioned embodiment, the pixel electrodes PX are formed on the upper surface of the third insulation film PAS. However, it is needless to say that, as shown in Fig. 9 (d), the pixel electrodes PX may be formed below the third insulation film PAS, that is, on the same layer as the drain signal lines DL. This is because that the substantially same advantageous effects can be obtained.

<<Video signal>>

Fig. 1 is a characteristic graph showing the center voltage which is changed in response to the magnitude of an amplitude of the video signal supplied to the respective drain signal lines DL of the liquid crystal display device according to the present invention and corresponds to Fig. 12 (b).

In the characteristic graph shown in Fig. 1, the amplitude of the video signal is taken on an axis of abscissas such that the amplitude assumes a minimum value at the left side in the drawing and a maximum value at the right side in the drawing and the center voltage of the video signal is taken on an axis of ordinates. Here, the center voltage of the video signal means an average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the video signal.

The center voltage of the video signal, first of all, assumes a certain value "a" when the amplitude of the video signal assumes the minimum value and is increased corresponding to the increase of the amplitude of the video signal to a first value thus assuming a certain value "b". Then, the center voltage of the video signal is decreased corresponding to the increase of the amplitude of the video signal to a second value. Then, when the center voltage of the video signal arrives at a certain value "c", the center voltage of the video signal is increased to reach the certain value "a" or a value which is close to the value "a". In other words, the center voltage of the video signal at the minimum amplitude value is set to

the proper center voltage at the maximum amplitude value and the center voltage of the video signal at the maximum amplitude value is set to the proper center voltage at the minimum amplitude value.

Basically, the characteristic graph shown in Fig. 1 is similar to the characteristic graph shown in Fig. 12 (a) with respect to a point that the center voltage of the video signal is decreased corresponding to the increase of the signal amplitude of the video signal. However, the characteristic graph of Fig. 1 differs from the characteristic graph shown in Fig. 12 (a) with respect to a point that the center voltage of the video signal is increased within a fixed range A starting from a point of time that the signal amplitude of the video signal assumes the minimum value (a range from the minimum value to the first value) and within a fixed range B from a point of time immediately before a point of time that the signal amplitude assumes the maximum value to the point of time that the signal amplitude assumes the maximum value (a range from the second value to the maximum value).

The reason that the above-mentioned characteristic graph is adopted is as follows. As shown in Fig. 12 (a), when the center voltage of the video signal is increased as it is with respect to the reference signal applied to the counter electrode corresponding to the decrease of the signal amplitude of the video signal, the difference between the center voltage of the

video signal at the minimum amplitude and the center voltage of the video signal at the maximum amplitude becomes relatively large. The characteristic graph shown in Fig. 1 is adopted to decrease this difference. By decreasing this difference, it is possible to enhance the response speed at the time of switching from white to black and black to white which are most important in the response time of the liquid crystal display device.

In this case, the reduction of image retention which is an advantageous effect of the characteristics shown in Fig. 12 (b) with respect to the characteristics shown in Fig. 12 (a) can be also maintained in this embodiment. This is because that also with respect to the characteristics of the video signal shown in Fig. 12 (b), there arises a phenomenon that the image retention is hardly observed in the vicinity of white and black excluding colors of intermediate tones.

That is, Fig. 2 shows a B (brightness)-V (voltage) curve of the liquid crystal in use. Although the change of brightness in response to the change of voltage is sensitive in portions except for portions where the amplitude of the video signal assumes the minimum value and the maximum value, the change of brightness becomes relatively insensitive to the change of voltage in the vicinity of the portions where the amplitude of the video signal assumes the minimum value and the maximum value.

In view of the above, the image retention is hardly recognized in the vicinity of the portions where the amplitude of the video signal assumes the minimum value and the maximum value (in other words, the range from the minimum value to the first value and the range from the second value to the maximum value).

Here, Fig. 2 is a graph in which the amplitude of the video signal is taken on an axis of abscissas and the brightness is taken on an axis of ordinates, wherein the liquid crystal in use is liquid crystal for a so-called normally white mode in which a white display is performed in a state that a voltage is not applied to the liquid crystal. However, with respect to the phenomenon that the image retention is hardly observed in the vicinity of white and black except for colors of intermediate tones, the circumstances are exactly same also with respect to a so-called normally black mode.

Fig. 3 is a characteristic graph showing another embodiment of the center voltage which is changed in response to the magnitude of amplitude of the video signal supplied to the respective drain signal lines DL of the liquid crystal display device according to the present invention and corresponds to Fig. 1.

A point which makes this characteristic graph different from the characteristic graph shown in Fig. 1 lies in that an average value "a" of the positive-side gray scale voltage and

the negative-side gray scale voltage of the video signal at the minimum signal amplitude of the video signal is set smaller than a value "c" of a starting point of the increase of the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the video signal in the vicinity of the maximum signal amplitude of the video signal.

Further, another point which makes this characteristic graph different from the characteristic graph shown in Fig. 1 lies in that an average value "d" of the positive-side gray scale voltage and the negative-side gray scale voltage of the video signal at the maximum signal amplitude of the video signal is set smaller than a value "b" of an arrival point of the increase of the average value of the positive-side gray scale voltage and the negative-side gray scale voltage of the video signal in the vicinity of the minimum signal amplitude of the video signal.

Due to such a constitution, compared to the characteristics of the video signal shown in Fig. 1, the superposition of DC voltages after switching of white and black can be reduced more effectively and hence, it is possible to achieve an advantageous effect that the response speed can be enhanced.

Here, in the above-mentioned graphs shown in Fig. 1 and Fig. 3, the signal amplitude of the video signal is taken on the axis of abscissas. However, it is possible to obtain the

substantially same advantageous effects even when the signal amplitude is replaced with the display gray scale.

<<relationship among video signal, reference signal and gate signal>>

Fig. 4 is a timing chart showing the video signal, the reference signal and the scanning signal supplied to the pixels.

In Fig. 4, time is taken on an axis of abscissas and a potential is taken on an axis of ordinates. First of all, the gate signal GV is supplied to the first-line gate signal line GL, for example. In this case, the gate signal GV has a gate ON voltage GV (H) and a gate OFF voltage GV (L) and the first-line gate signal line GL is selected in response to a pulse of the gate ON voltage GV (H). Due to such a selection, the thin film transistors TFT which adopt the first-line gate signal line GL as the gate electrodes assume the ON state and hence, the pixels which include the thin film transistors TFT in the ON state, that is, the respective pixels of the row of the first-line pixels which are arranged close to the given gate signal line GL and are arranged along the longitudinal direction of the given gate signal line GL assume a state in which the pixels receive the video signal DV via the corresponding drain signal line DL.

The supply of the video signal DV to the respective pixels of the pixel row is outputted in conformity with the selection timing of the gate signal line GL. In this case, the video

signal DV has the positive-side gray scale voltage (positive-polarity voltage) DV (U) and is supplied to the pixel electrode PX of the pixel by way of the thin film transistor TFT. Here, the positive-side gray scale voltage (positive-polarity voltage) DV (U) implies that the pixel electrode PX assumes the positive-polarity voltage with respect to the reference signal Vcom which is supplied to the counter electrode CT of each pixel.

Then, in the next operation, other gate signal line GL different from the above-mentioned given gate signal line GL, for example, the second-line gate signal line GL which is arranged close to the above-mentioned given gate signal line GL is selected, and the video signal DV is supplied to the respective pixels of the second-line pixel row which is arranged along the selected gate signal line GL. This video signal DV has the negative-side gray scale voltage (negative-polarity voltage) DV (L). The negative-side gray scale voltage (negative-polarity voltage) DV (L) assumes the negative-polarity voltage with respect to the reference signal Vcom supplied to the counter electrodes CT of the respective pixels.

That is, the video signal DV is supplied sequentially in conformity with the timing for supplying the scanning signal GV to the gate signal lines GL which are sequentially selected, wherein the polarity of the video signal DL is inverted for

every supply.

After the respective gate signal lines GL in one frame are all selected in this manner, the gate signal lines GL are sequentially selected in the substantially same manner in the next frame.

In this case, at a point of time that the above-mentioned first-line gate signal line GL is selected, the video signal DV which is supplied to the respective pixels of the first-line pixel row arranged along the gate signal line GL has the negative-side gray scale voltage (negative-polarity voltage) DV (L).

<<Gray scale voltage>>

The video signal DV is outputted in conformity with the timing of sequential supplying of the scanning signal, for example such that positive-side gray scale voltage (positive-polarity voltage) DV (U) and the negative-side gray scale voltage (negative-polarity voltage) DV (L) are alternately repeated. However, the video signal DV shown in Fig. 4 is indicated such that, for the sake of brevity of the explanation, the voltage value of the positive-side gray scale voltage (positive-polarity voltage) DV (U) and the voltage value of the negative-side gray scale voltage (negative-polarity voltage) DV (L) are fixed.

However, provided that these gray scale voltages are formed of a gray scale voltage, these gray scale voltages are

applied to the pixel electrodes PX having the voltage values corresponding to display colors of the pixels.

Fig. 5 shows a resistance voltage divider circuit which is provided at a final stage of a gray scale generating circuit incorporated in the above-mentioned video signal drive circuit He.

In the drawing, between a terminal TM1 to which a low-voltage-side reference voltage V0 is supplied and a terminal TM2 to which a high-voltage-side reference voltage Vmax is supplied, for example, seven resistances R1, R2, R3, … , R6, R7 are sequentially connected in series from the above-mentioned terminal TM1 side.

Then, voltages respectively having divided voltage values are supplied from connection points of respective resistances including the above-mentioned respective terminals TM1, TM2. That is, the voltage V1 is supplied from the terminal TM1, the voltage V2 is supplied from the connection point of the resistance R1 and the resistance R2, the voltage V3 is supplied from the connection point of the resistance R2 and the resistance R3, … , the voltage V7 is supplied from the connection point of the resistance R6 and the resistance R7, and the voltage V8 is supplied from the terminal TM2.

Among these voltages, the voltages V1 to V4 are taken out as the negative-side gray scale voltages (negative-polarity voltages) DV(L) and the voltages V5 to V8 are taken out as the

positive-side gray scale voltages (positive-polarity voltages) DV(U).

With respect to these gray scale voltages, in response to gray scale data for making given pixels perform a display among image data inputted to the liquid crystal display device, any one of the voltages V5 to V8 is selected when the gray scale voltage is inverted to the positive side and one of the voltages V1 to V4 is selected when the gray scale voltage is inverted to the negative side and, thereafter, is supplied to the drain signal line DL.

Here, although the resistance voltage divider circuit shown in Fig. 5 uses seven resistances, for example, the number of resistances is not limited. That is, the respective outputs may be further divided using resistances to obtain the finer division of gray scales and it is needless to say that the resistance voltage divider circuit can have such a constitution.

<< Relationship between center voltage and display gray scales of video signal >>

Fig. 6 is a graph showing the relationship between the center voltage CV of the video signal DV and the display gray scale of the video signal DV.

In Fig. 6, the display gray scale of the video signal DV is taken on an axis of abscissas in a state that the gray scale assumes the minimum value at the left side and the maximum value at the right side, while the voltage of the video signal

is taken on an axis of ordinates.

The center voltage of the video signal DV takes the change characteristics shown in the above-mentioned Fig. 1, wherein the center voltage firstly takes the value CV1 when the display gray scale is minimum and is increased corresponding to the increase of the display gray scale to a certain extent and assumes the value CV2. Then, the center voltage of the video signal DV is decreased corresponding to the subsequent increase of the display gray scale and assumes the value CV3 immediately before the maximum display gray scale and takes the value CV4 when the display gray scale becomes maximum.

With respect to this center voltage, the positive-side gray scale voltage (positive-polarity voltage) DV(U) is set such that the positive-side gray scale voltage DV(U) is increased sequentially along with the increase of the display gray scale, wherein the positive-side gray scale voltage DV(U) sequentially assumes V5, V6, V7 and V8 over a range from the minimum value to the maximum value of the pixel display gray scale. Further, with respect to this center voltage, the negative-side gray scale voltage (negative-polarity voltage) DV(L) is also set such that the negative-side gray scale voltage DV(L) is increased sequentially along with the increase of the display gray scale, wherein the negative-side gray scale voltage DV(L) sequentially assumes V4, V3, V2 and V1 over a range from the minimum value to the maximum value of the pixel display gray scale. In view

of the above, by setting the respective resistances R1, R2, R3, … , R6, F8 of the resistance voltage divider circuit shown in Fig. 5 to given values respectively and by allowing the respective gray scale voltages V1, V2, V3,… V7, V8 obtained based on these resistances to have the relationship shown in Fig. 6, it is apparent that the change characteristics of the center voltage of the video signal DV is also expressed as shown in Fig. 6.

Fig. 7(a) shows a case in which the respective resistances of the resistance voltage divider circuit shown in Fig. 5 are set such that R1=1Ω, R2=8Ω, R3=2Ω, R4=1Ω, R5=15Ω, R6=1Ω and R7=15Ω.

Fig. 7(b) shows a case in which the high-voltage-side reference voltage Vmax is set to 5.00V and the low-voltage-side reference voltage V0 is set to 0.20V in the resistance voltage divider circuit shown in Fig. 5, wherein the respective voltages divided by the resistances having the above-mentioned resistance values are set such that V8=5.00V, V7=3.33V, V6=3.21V, V5=1.54V, V4=1.42V, V3=1.20V, V2=0.31V, V1=0.20V.

Fig. 7(c) show the center voltages calculated based on the respective voltages obtained in Fig. 7(b), wherein the center voltages CV are set such that CV1=1.48V, CV2=2.21V, CV3=1.81V, CV4=2.60V. Here, CV1 is the average value of the above-mentioned voltages V5 and V4, CV2 is the average value of the above-mentioned voltages V6 and V3, CV3 is the average

value of the above-mentioned voltages V7 and V2, and CV4 is the average value of the above-mentioned voltages V8 and V1.

Embodiment 2.

Fig. 10 is a plan view showing another embodiment of the pixel of the liquid crystal display device according to the present invention and corresponds to Fig. 9(a).

The constitution which makes this embodiment different from the embodiment shown in Fig.9(a) lies in the constitution of the pixel electrode PX. That is, in this embodiment, the pixel electrode PX has an end portion thereof at a side opposite to the side where the pixel electrode PX is connected to the thin film transistor TFT extended to and superposed to another gate signal line GL which is arranged with the pixel electrode PX sandwiched between another gate signal line GL and the gate signal line GL which drives the thin film transistor TFT, and a capacitive element Cadd is formed on the superposed portion.

Due to such a constitution, the pixel can have both of the capacitive element Cstg and the capacitive element Cadd. It is needless to say that the pixel may be configured to have only the capacitive element Cadd without forming the capacitive element Cstg.

Embodiment 3.

Fig. 11 is a plan view showing another embodiment of the pixel of the liquid crystal display device according to the present invention. In the above-mentioned embodiments of the

pixel, the pixel electrode PX and the counter electrode CT are formed at the transparent substrate SUB1 side and the optical transmissivity of the liquid crystal is controlled by the electric field which is generated between these electrodes and has the component substantially parallel to the surface of the transparent substrate SUB1.

However, with respect to the pixel shown in Fig. 11, the counter electrode CT (not shown in the drawing) is formed on a liquid-crystal-side surface of the transparent substrate SUB2 which is arranged to face the transparent substrate SUB1 in an opposed manner with the liquid crystal therebetween in common with the respective pixels, wherein the optical transmissivity of the liquid crystal is controlled by the electric field which is generated between the counter electrode CT and the pixel electrodes PX and has the component perpendicular to the surface of the transparent substrate SUB1.

The pixel electrode PX is formed on the substantially whole area of the pixel region. By forming both of the pixel electrode PX and the counter electrode CT using a transparent conductive film such as ITO or the like, it is possible to observe the optical transmissivity of the liquid crystal with naked eyes.

Here, a portion of a periphery of the pixel electrode PX is formed in a superposed manner on another gate signal line GL which is arranged such that the pixel electrode PX is

sandwiched between another gate signal line GL and the gate signal line GL which drives the thin film transistor TFT connected to the pixel electrode PX, and a capacitive element Cadd is formed at the superposed portion.

The above-mentioned respective embodiments may be used in a signal form or in combination. This is because that the advantageous effects of the respective embodiments can be obtained in a single form or synergistically.

As can be clearly understood from the foregoing explanation, according to the liquid crystal display device of the present invention, it is possible to enhance the response speed of the display device.

(In the drawings)

(Fig. 1)

SIGNAL AMPLITUDE OF VIDEO SIGNAL

MAXIMUM

MINIMUM

CENTER VOLTAGE OF VIDEO SIGNAL

(Fig. 2)

SIGNAL AMPLITUDE OF VIDEO SIGNAL

MAXIMUM

MINIMUM

BRIGHTNESS

(Fig. 3)

SIGNAL AMPLITUDE OF VIDEO SIGNAL

MAXIMUM

MINIMUM

CENTER VOLTAGE OF VIDEO SIGNAL

(Fig. 4)

POSITIVE-POLARITY WRITING

NEGATIVE-POLARITY WRITING

(Fig. 5)

HIGH-VOLTAGE-SIDE REFERENCE VOLTAGE

LOW-VOLTAGE-SIDE REFERENCE VOLTAGE

(Fig. 6)

RELATIONSHIP BETWEEN DISPLAY GRAY SCALE AND VIDEO SIGNAL VOLTAGE

DISPLAY GRAY SCALE

MAXIMUM

MINIMUM

VOLTAGE OF VIDEO SIGNAL

SIGNAL VOLTAGE OF VIDEO SIGNAL

(Fig. 7)

RESISTANCE SET VALUE

VOLTAGE VALUE

CV VOLTAGE VALUE

(Fig. 12(a))

SIGNAL AMPLITUDE OF VIDEO SIGNAL

MAXIMUM

MINIMUM

CENTER VOLTAGE OF VIDEO SIGNAL

(Fig. 12(b))

SIGNAL AMPLITUDE OF VIDEO SIGNAL

MAXIMUM

MINIMUM

CENTER VOLTAGE OF VIDEO SIGNAL